



Department of Electrical Engineering and Computational Sciences
EENG 284 – Digital Design
Spring 2017

Instructor	TA
Vibhuti Dave BB 314C, 303-273-3670 vdave@mines.edu Office Hours MW: 8 – 9 AM and 3 – 3:30 PM T: 9 – 10 AM F: 10 – 11 AM	Gaurav Teotia BB 305 gauravteotia@mymail.mines.edu Office Hours MW: 2:30 – 3:30 PM Location: TBD

Pre-requisite: CSCI 261 or equivalent

Co-requisite EENG 281 or equivalent

Course Description

The course covers fundamentals of digital logic design. Design of combinational and sequential logic circuits, field programmable gate arrays, hardware description languages, and computer-aided design (CAD) tools will be studied. Laboratory component introduces simulation and synthesis software and hands-on hardware design.

Course Objectives

At the end of this course, student should

- Be able to represent and manipulate numbers in binary two's complement number system, and convert numbers between different positional number systems. Be able to do negation and addition in the two's complement number system, and detect overflow.
- Carry out transformations of Boolean algebra expressions, using the theorems of Boolean algebra and Karnaugh maps. The student can find the minimal sum-of-products (SOP) and product-of-sums (POS) expressions, and create a corresponding circuit from AND, OR, NAND, and NOR gates
- Design basic combinational building blocks such as adders, multiplexers and decoders. Use building blocks to design small-scale systems.
- Analyze and design clocked synchronous state machines.
- Design moderately complex systems using datapath and control approach.
- Perform timing analysis on small-scale systems.
- Map simple functions onto field programmable gate arrays manually.
- Analyze and design digital systems of moderate complexity using contemporary technology methods, including field programmable gate arrays and CAD tools.
- Be able to write proper lab reports, communicating their objectives, approach, observations, and conclusions.

- Analyze the functional and electrical behavior of digital CMOS circuits. Given an NMOS or CMOS circuit diagram, the student can determine its logic function, using switch models for the transistors

Required Material

- Digital Design, by M. Morris Mano and Michael D. Ciletti, Fifth Edition, Pearson/Prentice-Hall.
- Basic i>clicker. <http://www.iclicker.com/>

Reference Material

- Digital Design and Computer Architecture by David Harris and Sarah Harris
- Fundamentals of Digital Logic with Verilog Design, by Brown and Vranesic, McGraw Hall, 2nd edition, 2008

Grading

The grade you receive in this course will be based on the following:

Homework	10%
Laboratory	18%
Clicker Questions	10%
3 Quizzes @ 4% each	12%
2 Exams @ 12.5% each	25%
Final Exam	25%
Total	100%

The grading scale that will be used for this course:

A (93+)	A ⁻ (93- to 90+)	
B ⁺ (90- to 87+)	B (87- to 83+)	B ⁻ (83- to 80+)
C ⁺ (80- to 77+)	C (77- to 73+)	C ⁻ (73- to 70+)
D ⁺ (70- to 67+)	D (67- to 63+)	D ⁻ (63- to 60+)
F (60-)		

Attendance and Make Up

- Excessive absences will result in a lowered and possibly failing grade.**
- Any short quizzes given during class may only be made up if you have a formal excused absence. Last minute excuses will NOT be accepted.

- Exam and quiz dates are final. One week notice is required to schedule a make-up in case of a schedule conflict.
- There will be NO make up for clicker questions given during class.

Class Policies and Guidelines

- Skeleton lecture handouts will be provided in every class.
- **All cell phones need to be turned off for the duration of class.** After the first time you are seen using a cell phone, you will be required to turn it in at the beginning of every class for the rest of the semester. Do not take pictures of notes on the board. **Be active and physically take notes in class.**
- **You can use a laptop/tablet for note-taking purposes only.**
- **Lab attendance is mandatory** and you will stay in lab and work on the experiment for the entire duration of lab. You are required to be on time and are not allowed to leave early. **Penalty for arriving late, leaving early or an absence is 30% of that lab grade.**
- All homework assignments need to be turned in **at the beginning of class** on the dates they are due. **Late homework will NOT be accepted.**
- Lab reports need to be handed to the TA on the due date when you meet for lab. **Late lab reports will NOT be accepted.**
- Assignments need to be done individually. Do NOT copy. Group work is encouraged but the final result should be your work.
- You will receive a failing grade on the assignment if you have violated academic integrity. This includes copying from the Internet.
- In case you fail to attend class; it is your responsibility to get notes on the material covered in class.
- **Lecture notes, homework assignments, homework solutions will be posted on Canvas.**
- **Grades will be posted on Canvas. Please keep track of your grade on Canvas.**
- **We will use Piazza as a resource to get questions answered. If you have question regarding any material in class, or homework assignments, please post your questions on Piazza first.**
- **Please register your clickers with your usernames.** For example, my username is vdave.
- Exam and quiz questions will be based on homework assignments AND problems done in class.
- All grading errors need to be corrected before the final grade is posted. Final grades will not be changed once posted.
- The final exam is comprehensive.
- We will be using hardware and software from Altera Corp in this class to learn the use of CAD tools and Field Programmable Gate Arrays (FPGAs).
- The Altera software, called Quartus II, is installed on the computers in the EE labs in Brown Hall (BB304, BB305).

- A free version is available from the Altera website, <http://www.altera.com/>. The version used is Quartus II 15.0. Please download this version.
- Students will work in teams of up to two people in the regularly scheduled lab sections.
- A single lab report from each team is due to the lab instructor within one week after the lab project is completed.

Disability Support

The Colorado School of Mines is committed to ensuring the full participation of all students in its programs, including students with disabilities. If you are registered with Disability Support Services (DSS) and I have received your letter of accommodations, please contact me at your earliest convenience so we can discuss your needs in this course. For questions or other inquiries regarding disabilities, I encourage you to visit disabilities.mines.edu for more information.

Colorado School of Mines Academic Dishonesty Policy

The consequences for academic dishonesty at the Colorado School of Mines are severe and can lead to expulsion. The CSM culture requires that you take responsibility for your education in a responsible manner and adhere to the academic dishonesty policy.

The policy on homework is that it is perfectly acceptable for groups to work on the homework together. However, all students must turn in individual homework (unless otherwise stated) and they must understand what they turn in. Copying of solutions without understanding them is not allowed; if a student copies a solution and cannot explain it adequately this is considered academic dishonesty. For computer exercises each student is expected to generate his/her own solution (i.e. one cannot simply copy another person's computer solution and modify it slightly to make it look like it is your own work).

For laboratories, again students can work in groups but must understand all aspects of the laboratory. Representation of calculated data (i.e. dry lab) as measurements is considered academic dishonesty.

During exams, students must do 100 percent of the work on their own.

Spring 2017 Exam and Quiz Calendar

Exam/Quiz	Date
Quiz 1	February 10 th 2017
Exam 1	February 17 th 2017
Quiz 2	March 17 th 2017
Exam 2	March 24 th 2017
Quiz 3	April 28 th 2017
Comprehensive Final Exam	TBA
