DRAM Bank Operation

Access Address:
(Row 0, Column 0)
(Row 0, Column 1)
(Row 0, Column 85)
(Row 1, Column 0)

Row address 0

Column address 05

Row Buffer CONFLICT!
The DRAM Chip

- Consists of multiple banks (2-16 in DRAM)
- Banks share command/address/data buses
- The chip itself has a narrow interface (4-16 bits per read)
DRAM Rank and Module

• Rank: Multiple chips operated together to form a wide interface

• All chips comprising a rank are controlled at the same time
  – Respond to a single command
  – Share address and command buses, but provide different data

• A DRAM module consists of one or more ranks
  – E.g., DIMM (dual inline memory module)
  – This is what you plug into your motherboard

• If we have chips with 8-bit interface, to read 8 bytes in a single access, use 8 chips in a DIMM
A 64-bit Wide DIMM (One Rank)
Multiple DIMMs

- **Advantages:**
  - Enables even higher capacity

- **Disadvantages:**
  - Interconnect complexity and energy consumption can be high

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**Diagram:**

- **Single Channel SDRAM Controller**
- **Mesh Topology**:
  - Addr & Cmd
  - Data Bus
  - Chip (DIMM) Select
DRAM Channels

• 2 Independent Channels: 2 Memory Controllers (Above)
Generalized Memory Structure
Generalized Memory Structure
The DRAM Subsystem
The Top Down View
DRAM Subsystem Organization

- Channel
- DIMM
- Rank
- Chip
- Bank
- Row/Column
The DRAM subsystem

“Channel”

DIMM (Dual in-line memory module)

Processor

Memory channel

Memory channel
Breaking down a DIMM

DIMM (Dual in-line memory module)
Breaking down a DIMM

DIMM (Dual in-line memory module)

Side view

Front of DIMM

Back of DIMM

Rank 0: collection of 8 chips

Rank 1
Breaking down a Rank

Rank 0

Chip 0
Chip 1

... Chip 7

Data <0:63>
Breaking down a Chip
Breaking down a Bank

Bank 0

Row-buffer

1B (column)

2kB

row 0

row 16k-1

...
DRAM Subsystem Organization

- Channel
- DIMM
- Rank
- Chip
- Bank
- Row/Column
Example: Transferring a cache block

Physical memory space

Channel 0

DIMM 0

Rank 0

Mapped to

64B cache block
Example: Transferring a cache block

Physical memory space

0xFFFF...F

... 64B cache block

0x40

0x00

Chip 0  Chip 1  Chip 7

Rank 0

Data <0:63>

<0:7>  <8:15>  <56:63>
Example: Transferring a cache block

Physical memory space

0xFFFF...F

... 0x40 0x00

64B cache block

Chip 0  Chip 1  ...  Chip 7

<0:7>  <8:15>  <56:63>

Data <0:63>

Row 0 Col 0

Rank 0
Example: Transferring a cache block

Physical memory space

0xFFFF...F

0x40

0x00

8B cache block

64B

Row 0
Col 0

Chip 0
Chip 1

<0:7>
<8:15>
<56:63>

8B

Data <0:63>

8B

Rank 0

Chip 7
Example: Transferring a cache block

Physical memory space

0xFFFF\ldots\text{F}

0x0FFF...F

0x40

0x00

8B cache block

64B

Row 0

Col 1

Chip 0

Chip 1

Chip 7

Rank 0

Data <0:63>

<0:7>

<8:15>

<56:63>
Example: Transferring a cache block

Physical memory space

Data <0:63>
Example: Transferring a cache block

A 64B cache block takes 8 I/O cycles to transfer.

During the process, 8 columns are read sequentially.