Programmable PFC Based Hybrid Multipulse Power Rectifier for Ultra Clean Power Application

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Abstract—A novel hybrid three-phase rectifier is proposed. It is capable of achieving high input power factor (PF) and low total harmonic current inputs distortion (THD). The proposed hybrid high power rectifier is composed by a standard three-phase six-pulse diode rectifier (Graetz bridge) with a parallel connection of single-phase Sepic rectifiers in each three-phase rectifier leg. Such topology results in a structure capable of programming the input current waveform and providing conditions for obtaining high input power factor and low harmonic current distortion. In order to validate the proposed hybrid rectifier, this work describes its principles, with detailed operation, simulation, experimental results, and discussions on power rating of the required Sepic converters as related to the desired total harmonic current distortion. It is demonstrated that only a fraction of the output power is processed through the Sepic converters, making the proposed solution economically viable for very high power installations, with fast investment payback. Moreover, retrofitting to existing installations is also feasible since the parallel path can be easily controlled by integration with the existing dc-link. A prototype has been implemented in the laboratory and it was fully demonstrated to both operate with excellent performance and be feasibly implemented in higher power applications.

I. INTRODUCTION

IN ORDER to improve the distribution of electrical energy and to provide agreement with the power quality standards, special rectifier structures have been currently used as front end energy processors. But three-phase diode-bridge rectifiers continue to be very popular in several industrial and rural applications, where an intermediate dc link provides energy for other electronic circuits. However, such standard diode-bridge rectifiers do not meet harmonic current content restrictions, as imposed by several international standards such as IEC 61000 and IEEE 519 [1]–[6]. Thus, expensive and bulky passive filters or complex power factor correction (PFC) and active filter structures must be installed to compensate the inherent harmonic current distortion. Therefore, in the past few years there has been a tremendous interest in achieving low harmonic current distortion in three-phase ac to dc converters, motivating the development of several front-end multipulse rectifier solutions [7]–[11].

Multipulse rectifiers have been typically applied in three-phase applications for mitigation of the input current harmonic content. However, these converters need magnetic circuits such as multiphase transformers, interphase transformers, current balancing transformers, or harmonic blocking transformers, resulting in customized equipment which are complex, heavy, bulky, and expensive [12]–[16]. In addition, elimination of interphase transformers is particularly desirable when there is preexisting harmonic voltage content in the three-phase power source. Such harmonic voltages cause fluctuations in the dc output voltage, leading to further design complexities [12]–[14], [17].

A simplified transformer concept for multipulse rectifier application was proposed in order to improve current sharing between two rectifiers [18] and eliminate the use of an interphase transformer. However, to compose the input line current waveform, a power transformer with a rating of 1.16P_{out} (where P_{out} is the nominal value of output power) was necessary. Such a device contributes for increased cost, weight, and size of the structure. In the same context, in [19] the authors proposed an active multipulse rectifier system using Boost converters to shape the input line current to sinusoidal waveform and to improve current sharing, without the use of an interphase transformer. In this case, a controlled dc output voltage is achieved through the use of two Boost converters processing 50% of the output power (P_{out}) and, a power transformer with a rating of 0.6169P_{out}, limiting its application and increasing the cost, weight, and size of the proposed structure.

A novel approach that overcomes such disadvantages is presented in this paper. The authors propose a new structure composed of a single-phase Sepic rectifier associated in parallel with each leg of a three-phase six-pulse diode rectifier resulting in a programmable input line current waveform structure. Thus, controlled rectifiers operating in parallel to a standard three-phase diode rectifier are proposed in contrast to expensive and complex schemes. The overall converter behaves as a current source controlled with a suitable strategy, i.e., the imposition of a suitable input line current waveform in order to provide THD of total harmonic distortion of current and high input power factor. The system is a programmable PFC based hybrid multipulse power rectifier (PFC–HMPR) deploying Sepic converters. The proposed structure is depicted in Fig. 1. It is a very compact structure and somewhat easy to implement when compared to the expensive and complex multipulse schemes. The proposed system is capable of providing ultra clean power without using multiphase transformers, interphase transformers, current balancing transformers, or harmonic blocking transformers. This new topology is described and analyzed in the next section.

It is important to emphasize that the proposed hybrid multipulse power rectifier deploying Sepic rectifiers in parallel to...
Fig. 1. New three-phase PFC hybrid multipulse power rectifier (PFC-HMPR).

II. FUNDAMENTAL PRINCIPLES

Fig. 1 shows the PFC–HMPR which is composed by a standard three-phase six-pulse diode rectifier, indicated in the block diagram as Rect—1, and single-phase Sepic rectifiers associated in parallel to each diode-bridge rectifier leg. It should be observed that non-isolated Boost rectifiers are not capable of imposing input current waveform when operating in parallel connection such as indicated in Fig. 1. Thus, the proposed system has single-phase Sepic rectifiers, which have been observed to have the capabilities to impose a desirable input line current waveform.

Fig. 2 shows the principle of constructing an input line current $i_{a(n)}$ through two components $i_{a3}$ and $i_{a2}$, obtained when the PFC–HMPR topology operates as a conventional three-phase 12-pulse rectifier, which is the focus of this paper.

The $I_{a2}$ current reference is the main controller of the overall characteristic of the final input line current waveform, as analyzed in Section IV. The proposed PFC-HMPR allows the improvement of the input line current $I_{a(0in)}$ by reducing its THD. It is important to notice that, only a fraction of the total output power is required to flow through the Sepic parallel circuits, supporting a competitive economic impact. It was experimentally observed that for the PFC-HMPR operating as a conventional 12-pulse rectifier, just about 20% of the total output power is processed by the Sepic rectifiers and a THD less than 14% in the input line current can be achieved. Besides, one can observe that a variety of harmonic content restrictions imposed by IEEE std 519–1992 can be easily meet by the PFC-HMPR presented in this paper, as one can see in Fig. 3. For example, if a controlled waveform as indicated in Fig. 3(b) is imposed through the Sepic parallel rectifiers, the input line current $i_{a(n)}$ will be composed of the combination of $i_{a3}$ and $i_{a2}$ with a very low THD (around 5%). In this case, the Sepic converters will supply about 45% of the rated power. In conclusion, the proposed PFC–HMPR is able to operate with a programmable THD in the input line current.
this flexibility is a very good characteristic of the proposed hybrid power rectifier system when compared to other multipulse rectifier structures.

Depending on the kind of application, the proposed hybrid rectifier can operate in accordance to the harmonic content restrictions of the input line current with the Sepic rectifiers processing just the minimum power. Therefore, the whole structure presents reduced cost, volume and, higher efficiency when compared to other multipulse schemes that use multi-phase transformers and interphase transformers, saving energy and attending the IEEE Std. 519–1992 as well. Moreover, the economical benefits of this new topology are extremely valuable for high power installations, because around 33% maximum value of rated power will be processed in the parallel circuits (Sepic rectifiers), in order to reduce the THD to a very low value (around 5%). This feature allows higher efficiency and payback in a very short time for the investment. Moreover, when used in retrofitting applications, the available total rated power will increase to 133% of the original output power, with obvious improvements on power quality. In this paper, the authors show the proposed PFC-HMPR operating as a conventional 12-pulse rectifier. The imposition of a sinusoidal input current waveform is under progress and will be reported in the future.

III. MOTIVATION TO USE A SEPIC CONVERTER

Boost converters have been traditionally used as front-end wave shaping systems but, in order to be applied as parallel path of three-phase six-pulse diode bridge rectifier, non-isolated Boost converters are not suitable because during the period of time where the input line voltage of the three-phase power source is higher than the dc output voltage, the Boost current keep increasing even when the switch is open. In fact, when the Boost switch is open and the freewheeling diode is forward biased and connecting the path between Rect-2 and Rect-1, the Boost current flows through the diodes of the three-phase six-pulse rectifier bridge (Rect-1) and its control is lost, eventually impeding the desired current waveform composition. This is the main reason that non-isolated Boost converters are not suitable for being associated in parallel for the proposed multipulse hybrid power rectifier.

On the other hand, Sepic converters behave naturally as an input current source, allowing that the waveform of the input current can be imposed with a suitable control strategy. In contrast to the Boost converter behavior, when the switch $S_2$ is opened ($I_2$), the series capacitor of the Sepic converter assures, at any operating conditions, the isolation of those circuits and correspondent decrease of the current flow through the input inductor. Thus, the imposition of the input current does not strongly depend on the level of the output voltage $V_0$ (dc link voltage).

It should be emphasized that for isolated Boost converters fed through single-phase transformers, there is galvanic isolation, as shown in Fig. 4. As a result, such structure is able to replace Sepic converters, but with the obvious drawbacks (volume, weight and cost) of requiring extra magnetic devices. The authors discuss in [20] the implementation with Boost converters, as shown in Fig. 4. The Boost current is confined to the secondary winding circuit and the dc link voltage is kept with average value approximately equal to the peak line voltage value approximately. This structure is able to replace the Sepic converters because it can be assured that Boost current will be forced to return through the Boost circuit instead of the three-phase six-pulse rectifier bridge. Hence, the control of the Boost current is no longer lost resulting that the desired input line current waveform can be achieved. It is important to emphasize that, even using single-phase isolating transformers, the proposed PFC-HMPR deploying Boost converters is still more attractive than the multipulse rectifier structures presented in [18] and [19], as described in [20].

IV. PROPOSED CONTROL STRATEGY

The main control circuit objective is to impose the input line current at low THD and high input power factor for the proposed PFC–HMPR. Therefore, the control strategy must focus on establishing the best relationship between the input current $i_{a1}$ of the standard three-phase six-pulse diode bridge rectifier (Rect-1), and the input current $i_{a2}$ of the controlled Sepic
rectifiers (Rect-2), in order to achieve a desirable input line current THD. As example, if a twelve pulses ac current waveform is desired, the control strategy of the controlled Sepic rectifiers (Rect-2) can be established as shown in the diagram of Fig. 5.

In order to compose the waveform of the input line current $I_{an}(t)$, a sample of the input line-to-neutral voltage ($V_a$) must be rectified and compared with dc voltage levels in order to generate a synchronized square wave ($V_{REF}$) to impose the input Sepic current ($I_d$) depicted in Fig. 2. The voltage $V_{REF}$ is the reference current waveform and can be supplied either by analog or digital devices. It was found that, when operating as a conventional 12-pulse rectifier, the lowest input line current THD is achieved when the magnitude of the current $I_{an}(t)$ of Rect-2 is 33% of the magnitude of the current $I_{Rect-1}$ of Rect-1. Therefore, the reference voltage $V_{REF}$ must be multiplied by a fraction of the current $I_{Rect-1}$-1 providing a reference signal equal to $V_{REF} \times (k \times I_{Rect-1})$, where $k$ is equal to 1/3 of the dc current through the output inductor filter ($I_L$) of the three-phase six-pulse diode rectifier (Rect-1) for the minimum THD.

In order to generate a PWM reference signal, a sawtooth voltage waveform $V_S$ is added to the multiplier circuit signal. Finally, the PWM reference signal must be compared with the cur-
TABLE I
DESIGNED PARAMETERS AND USED SEMICONDUCTORS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Link Voltage</td>
<td>V_{dclink} = 295 V</td>
</tr>
<tr>
<td>Total output power</td>
<td>P_{out} = 3 kW</td>
</tr>
<tr>
<td>6-Pulse Diode Rectifier (Rect-1)</td>
<td>Sepic Rectifiers (Rect-2)</td>
</tr>
<tr>
<td>Input voltage, V_i (rms)</td>
<td>110 V</td>
</tr>
<tr>
<td>Output capacitor, C_i = 10 μF</td>
<td></td>
</tr>
<tr>
<td>Output inductors, L_i = 10 mH</td>
<td></td>
</tr>
<tr>
<td>Output inductor, L_{i2} = 5 mH</td>
<td></td>
</tr>
<tr>
<td>Three-phase Rectifier Bridge - Toshiba 30J6P41</td>
<td></td>
</tr>
<tr>
<td>Single-phase Rectifier Bridge - IR-KBPCI</td>
<td></td>
</tr>
<tr>
<td>12-pulse PWM control strategy</td>
<td></td>
</tr>
<tr>
<td>Switching frequency, f_s = 30 kHz</td>
<td></td>
</tr>
<tr>
<td>Output power, P_{out} = 2370 kW - 79%</td>
<td></td>
</tr>
<tr>
<td>Output power, P_{out } = 630 W - 21%</td>
<td></td>
</tr>
</tbody>
</table>

Fig. 7. Input currents i_nα (Sepic)—simulation result.

Fig. 8. Input current i_nβ (six-pulse diode rectifier)—simulation result.

current flowing through the inductor L_1 of Sepic converter (Rect-2) to generate the gate-drive signal for switch S_1. Hence, the current through the inductor L_1 will follow the imposed reference through a very simple PWM control strategy [21], [22].

A. Simulation Results

In order to analyze the operation of the proposed PFC-HMPR, a digital simulation was performed and then compared with experimental results. Table I shows the system specifications. A 12-pulse PWM control strategy was applied in order to control the proposed structure, imposing 12-pulse waveform in the line input currents. Thus, the proposed control shown in Fig. 5 was implemented, and used for simulation analysis. An open loop control strategy, following the principles depicted in Fig. 6 was implemented in PSPICE.

The simulation results for the input line current composition are portrayed in Figs. 7 and 8. Fig. 7 shows the input current I_nα from the controlled Sepic rectifier, considering highly dc inductive filters (L_{F1} and L_{F2}).

Fig. 9 shows the simulation of input voltage and current waveforms where it can be observed that a 12-pulse input current waveform was imposed in the input line current, resulting in a THD near to 13.7%, for nominal output power. Fig. 10 shows the frequency spectrum of the input line current, for rated load. The ripple voltage over the average nominal output voltage is depicted on Fig. 11.

The simulation studies supported the best relationship between the magnitudes of current I_{Rect-2} magnitude and current I_{Rect-1} to be about 33%. This relationship gives the lowest THD of 13.55% for a 12-pulse waveform in the line input current, as shown in Fig. 12. Fig. 13 shows the power rating of Rect-2 in relation to the total output power. Therefore, one can
observe that, processing only 15.29% of the total output power, less than 14% of THD in the line input current is achieved.

B. Experimental Results

After careful simulation study and analysis, a 3-kW three-phase PFC non-isolated multipulse hybrid power rectifier (PFC–HMPR) prototype was implemented and evaluated in laboratory, in order to validate the proposed structure. The experimental setup was built using analog and digital gate circuitry. Fig. 14 shows the electrical diagram of the implemented prototype and details of the electronic circuit used in the experimental setup to compose the input current of line A. It should be noticed that all implemented parameters and devices are the same from Table I. As one can observe in Fig. 14, a sample of the input voltage is rectified and compared with two dc voltages levels for the pulse generator circuit.

The outputs of the comparators are connected to an OR gate resulting a pulsed output voltage with width equal to $\pi/3$ rad and amplitude equal to the comparator supply voltage, and the reference current waveform is obtained. Therefore, the reference current signal is filtered and reduced to unity value in order to be applied to the input of the signal multiplier circuit. The signal multiplier circuit also receives a current signal of the six-pulse diode rectifier in order to generate a signal proportional to 1/3 of the current $I_{\text{Rect-1}}$. As a result, the reference current signal to be imposed at the Sepic rectifiers is obtained at the output of the multiplier circuit.

Finally, the PWM reference generator circuit receives the signal from multiplier circuit and, with a sawtooth waveform, provides the PWM reference current signal that is compared with the current through the inductor of Sepic rectifiers. Therefore, the driving command to the main Sepic switch is provided through the gate drive circuit.

The experimental results are shown from Figs. 15–18. They are related to phase A of the power system, corroborating the behavior of the analyzed simulation results; the other phases have similar performance.

Figs. 15–16 show the currents from the controlled Sepic rectifier and uncontrolled six-pulse diode bridge rectifier, respectively. These currents are responsible to perform the 12-pulse waveform in the input line current. The experimental line input
The experimental input line current frequency spectrum is shown in Fig. 18, where an experimental THD$_{1}$ of 14.7% was achieved, resulting in an input power factor (PF) equal 0.989, for rated load. It was verified that the power rating of the parallel Sepic rectifiers (Rect-2) was about 21% of the total output power, which is a very close match to the results obtained in the simulation analysis.

V. CONCLUSION

This paper introduced a novel three-phase hybrid power rectifier capable of achieving nearly unity input power factor with programmable input line current THD$_{1}$. The paper presented comprehensive analysis, evaluation and design of a system composed of single-phase Sepic rectifiers connected to each leg of a standard uncontrolled three-phase six-pulse diode rectifier. The parallel converters power rating is only a small fraction of the total output power supporting a competitive economic impact. Additional analyses were presented to determine the amount of power processed by the controlled rectifiers, in order to obtain a given (and desirable) total harmonic distortion in the input line current (THD$_{1}$). It was verified that for THD$_{1}$ less than 15% only 21% of the rated output power had to be processed by the Sepic rectifiers. Therefore, this proposed structure is recommended for high power installations, and retrofitting to existing installations is feasible since the parallel path can be easily controlled by integration with the existing dc-link. The proposed structure provided a multipulse ac input line current without phase-shift transformers, with simplified design and reduced cost. In addition to the converter analysis and simulation results, experimental results from a 3-kW prototype were presented, in order to validate the proposed structure and control strategy. The authors are working on further developments towards a fully digital programmable control (using DSP and FPGA devices) for the proposed converter.

REFERENCES


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