The timing diagram showing the timing detail for the register data and decoder is shown in Figure 1. The 64 bits are first loaded into the eight shift registers from digital pins PD 0..7. The current plane is then selected by the 3:8 decoder on digital pins PB 1..3, and the decoder is enabled by digital pin PB 4 thereby grounding the plane. The decoder is then disabled, the next 64 bits are loaded, and the next plane is grounded.

Figure 1: Timing diagram for shift register data, plane selection and decoder enable.